1. A method comprising:

generating a clock signal aligned relative to an edge of a strobe signal received from a transmitting device; and

latching one or more data signals received from the transmitting device using the clock signal.

2. The method of claim 1, wherein the generating the clock signal comprises substantially aligning an edge of the clock signal with an edge of a strobe signal and delaying the clock signal by a predetermined amount of time.

3. The method of claim 1, wherein the method comprises generating one or more latch control signals aligned relative to the clock signal; and

wherein the latching comprises latching one or more data signals received from the transmitting device with one or more latch control signals.

4. The method of claim 3, wherein the generating the clock signal comprises substantially aligning an edge of the clock signal with an edge of a strobe signal; and

wherein the generating one or more latch control signals comprises substantially aligning an edge of one or more latch control signals with an edge of the clock signal and delaying one or more latch control signals by a predetermined amount of time.

5. The method of claim 3, wherein the latching comprises latching a first set of a plurality of data signals with a first latch control signal and latching a second set of a plurality of data signals with a second latch control signal.

6. The method of claim 1, comprising receiving from the transmitting device a strobe signal defining a pulse having a first edge associated with a first set of one or more data signals and a second edge associated with a second set of one or more data signals.

7. The method of claim 1, comprising transmitting a request to the transmitting device to receive a strobe signal for alignment of the clock signal after a strobe signal has not been received for a predetermined time interval.

8. An apparatus comprising:

clock generation circuitry to generate a clock signal aligned relative to an edge of a strobe signal received from a transmitting device;

control signal generation circuitry to generate one or more latch control signals aligned relative to an edge of the clock signal; and

latching circuitry to latch one or more data signals received from the transmitting device with one or more latch control signals.

9. The apparatus of claim 8, wherein the clock generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal and circuitry to delay the clock signal by a predetermined amount of time.

10. The apparatus of claim 8, wherein the clock generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal; and

wherein the control signal generation circuitry comprises circuitry to substantially align an edge of one or more latch control signals with an edge of the clock signal and circuitry to delay one or more latch control signals by a predetermined amount of time.

11. The apparatus of claim 8, wherein the clock generation circuitry is to receive from the transmitting device a strobe signal defining a pulse having a first edge associated with a first set of one or more data signals and a second edge associated with a second set of one or more data signals.

12. The apparatus of claim 8, wherein the latching circuitry comprises a first latch to latch a first set of a plurality of data signals with a first latch control signal and a second latch to latch a second set of a plurality of data signals with a second latch control signal.

13. The apparatus of claim 8, comprising clock alignment control circuitry to request to receive a strobe signal for alignment of the clock signal.

14. The apparatus of claim 13, wherein the clock alignment control circuitry comprises a counter to maintain a count to track time and a comparator to compare the count to a predetermined time interval.

15. An apparatus comprising:
means for aligning a clock signal with a strobe signal; and
means for latching one or more data signals using the clock signal.

16. The apparatus of claim 15, comprising means for delaying the clock signal.

17. The apparatus of claim 15, comprising means for generating one or more latch control signals aligned with the clock signal.

18. The apparatus of claim 17, comprising means for delaying one or more latch control signals.

19. The apparatus of claim 15, comprising means for requesting a strobe signal to align the clock signal.

20. A system comprising:
one or more processors;
one or more memory modules; and
a memory controller coupled to one or more processors and to one or more memory modules, the memory controller having data signal reception latch control using a clock aligned relative to a strobe signal received from a memory module.

21. The system of claim 20, wherein the memory controller comprises respective latch control circuitry for each of a plurality of strobe signal lines for one or more memory modules, each latch control circuitry comprising clock generation circuitry to generate a clock signal aligned relative to an edge of a strobe signal received from the respective strobe signal line and control signal generation circuitry to generate one or more latch control signals aligned relative to an edge of the clock signal.

22. The system of claim 21, wherein the clock generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal and circuitry to delay the clock signal by a predetermined amount of time.

23. The system of claim 21, wherein the clock generation circuitry comprises circuitry to substantially align an edge of the clock signal with an edge of a strobe signal; and

wherein the control signal generation circuitry comprises circuitry to substantially align an edge of one or more latch control signals with an edge of the clock signal and circuitry to delay one or more latch control signals by a predetermined amount of time.

24. The system of claim 21, wherein the memory controller comprises latching circuitry to latch one or more data signals received from one or more memory modules with one or more latch control signals.

25. The system of claim 20, wherein the memory controller comprises respective clock alignment control circuitry for each of a plurality of strobe signal lines for one or more memory modules, each clock alignment control circuitry to request to receive a strobe signal over the respective strobe signal line for alignment of a clock signal.

26. The system of claim 20, wherein one or more memory modules comprise double data rate dynamic random access memory (DDR DRAM).